IN THE U.S. PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/005,766
Applicant	:	Antti Ruha et al.
Filed	:	November 2, 2001
TC/AU	:	2618
Examiner	:	Tran, Pablo N
Docket No.	:	872.0100.U1(US)
Customer No.	:	29683
Title	:	MULTI-MODE I/O CIRCUITRY SUPPORTING LOW INTERFERENCE SIGNALING SCHEMES FOR HIGH SPEED DIGITAL INTERFACES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. § 1.131

1. We, Antii Ruha, Tarmo Ruotsalainen, and Jussi-Pekka Tervaluoto hereby attest that we are the joint and first inventors of the invention described and claimed in the above-referenced patent application now pending before the U.S. Patent Office.

2. We conceived of the invention as described in Exhibit A at least as early as April 19, 2001 and the inventive activity occurred in a US/NAFTA/WIPO country. Exhibit A is our invention report which was presented internally for Evaluation by Nokia in Oulu, Finland at least by April 19, 2001.

3. We hereby attest that the Exhibit cited herein is a true copy. We hereby acknowledge that the statements made herein are true or are made on information and belief that is believed to be true. We further acknowledge that any willful false statements are punishable by fine or imprisonment, or both, in accordance with 18 U.S.C. § 1001; and that such false statements may jeopardize the validity of any patent that may issue from the application to which this Declaration pertains.

Respectfully Submitted,

Antti Ruha

30th Dec 2007

Antii Ruha

Date

S.N.: 10/005,766
Art Unit: 2618

Tarmo Ruotsalainen — 28-Nov-2007
Date

Jussi-Pekka Tervaluoto — 28-Nov-2007
Date

NOKIA

CONFIDENTIAL

INVENTION REPORT

Title of invention: Multimode I/O circuitry supporting low interference signaling schemes for high speed digital interfaces.	INVENTION REPORT RECEIVED Code: Patent Committee: Place: Date: Signature:
THE DESCRIPTION OF THE INVENTION MUST BE ATTACHED	

Inventor's name, employee number, title and nationality: *)	Home Address: *)	Business Unit and cost centre:
Antti Ruha, 10022549, Research Manager	Uistintie 21A, 90550 Oulu, Finland	NMP/Oulu, BB RTT, 1016450
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Phone: *) +358-50-3200 109 | Fax: *)

The invention becomes public on:

I am/ We are the sole/ and original inventor(s) of this invention.

The company may, by virtue of applicable legislation, be entitled to full or partial rights to the invention. I/ We acknowledge my/ our obligation to sign as inventor(s) all documents that may be required for protecting the invention in different countries.

Applicable to inventions made by inventors employed in FI, DK, DE and SE only.

Unless the inventor requests the Invention Report to be responded to within four (4) months from the date this Invention Report is received or such other period as the mandatory provisions of the applicable local law may otherwise require, the inventor consents to the right of the employer to use a reasonable period of time for the evaluation of the invention. A reasonable period of time may exceed four (4) months.

☒ *I / We request that the Invention Report be responded to within four (4) months.*

Date:
Signature(s) of Inventor(s):

*) See the instructions

I have read and understood the invention described in this Invention Report

Date:
Signature of Manager

EXHIBIT A

INSTRUCTIONS FOR COMPLETING THE INVENTION REPORT

This Invention Report form is used in cases where an invention has been made by an employee of the Company. This Invention Report is confidential. Only the Patent Department may make copies of signed Invention Reports in order to request opinions or reply to the inventor(s).

The inventor completes the Invention Report and the description of the invention. The inventor does not fill in the 'Invention Report received' field. This field is filled in by the Patent Department. The Invention Report must have the names of all the inventors and their home addresses. If there is not enough space for all the names, addresses etc, please write them on a separate attachment. The first mentioned inventor is assumed to be the contact person in matters concerning the Invention Report. In the fields of office address, phone and fax, please fill in the contact person's information. Fill in the project field, if the invention is made in a project. The original Invention Report is signed by all inventors. Each page of the original Invention Report is signed by a Manager. In case it is difficult to obtain Manager's signature your Patent Department will take care of it.

It is suggested that the Invention Report and the description of the invention should be filled in as thoroughly as possible. If drawings or other kind of information cannot be attached to this form, they should be delivered separately.

The signed Invention Report is given directly to the local or business unit's Patent Department. Invention Report should also be sent by E-mail to the Patent Department. The Patent Engineer will inform the inventor of receiving the Invention Report. The Patent Engineer will obtain any expert opinions needed to properly evaluate the invention, will procure the Company's decision and inform the inventor accordingly.

I have read and understood the invention described in this Invention Report

Date:
Signature of Manager

DESCRIPTION OF THE INVENTION

Please, describe your invention in the following order. You can enclose the drawings on a separate document.

1. Field and background of the invention

Modern telecommunications systems transmit, receive, store and retrieve ever increasing amouts of data. The transmission of information between integrated circuits (IC) in complex systems requires that the signaling scheme and input-output (I/O) circuitry

- is capable of high speed operation
- generates little disturbances
- is tolerant to interferences
- consumes little power
- occupies little area

Furthermore, it would be highly desirable from the usability point of view that the scheme and circuitry would

- support different supply voltages in the transmitter and receiver
- be backward and forward compatible
- be capable of multimode operation

Commonly used CMOS digital signaling using single-ended voltage mode signals with rail-to-rail levels and fast edges generates lots of disturbances and interferences, and can limit the maximum usable data rates or seriously affect the performance of the system. The disturbances are especially detrimental in radiocommunications systems, where the analog signals can be extremely weak.

One way to reduce the generation of disturbances is to use analog signaling between ICs. This, however, means that both the transmitter and receiver ICs have to contain analog circuitry, e.g. ADCs and DACs. The incorporation of any analog circuitry in otherwise digital ICs is problematic, because digital ICs are usually implemented in highly optimized digital processes. In these digital deep sub-micron CMOS processes

- maximum supply voltages are going down
- analog properties of active devices, such as noise and early voltage, are getting worse and worse
- variety of available devices is limited, especially passive devices are available only with expensive extra process steps

Analog signaling and the associated analog circuitry (e.g. ADCs/DACs) in digital ICs may lead to prohitively large area and power hungry solutions. Furthermore, implementing analog or mixed signal circuitry on large digital ICs

- makes design and testing more difficult, time consuming and expensive
- and therefore increases risks and delays

Moreover, the price per silicon area in deep sub-micron CMOS processes is getting higher all the time. As the area of analog circuitry does not scale down at the same rate, analog circuitry on digital ICs is getting increasingly expensive.

From the above one can derive that

- it is often advantageous that large digital ICs contain only digital circuitry
- RF, analog and mixed signal circuitry should be placed in a separate chip implemented with a more appropriate process technology
- signaling between ICs should be optimized instead

Therefore is of utmost importance to develop efficient and preferentially signaling schemes, which allow optimal system partitioning.

2. A summary of the invention

This invention report describes multimode I/O circuitry supporting low interference signaling schemes for high speed digital interfaces between ICs in for example mobile communications systems. The proposed I/O circuitry supports single-ended and differential current mode, low swing voltage mode and CMOS signaling, and the operation mode of the presented receiver and transmitter circuits can be selected with a few control bits. The proposed I/O circuitry utilizes only standard MOS transistors and can therefore be implemented using any CMOS or BiCMOS technology.

From the interference point of view probably the best signaling scheme is differential current mode signaling. The proposed I/O circuitry supports this preferred mode of operation, but both the receiver and transmitter circuitry can also be used with for example existing CMOS level I/O circuitry, which is important from point of view of compatibility with existing and emerging systems. For example, a receiving IC equipped with the proposed receiver I/O circuitry (say DCT5 BB IC) could communicate with transmitting circuits from the same (DCT5 EM IC) or different generation (say DCT4 EM IC).

3. Describe the problem which the invention overcomes

The general problem is how to transmit increasing amounts of data between ICs without compromising or deteriorating the performance of the systems with the interferences and disturbances associated with high speed digital data links.

The invention overcomes the following specific technical problems

- Compatibility issues: The proposed I/O circuitry supports single-ended and differential current mode, low swing voltage mode and CMOS signaling, and the operation mode of the presented receiver and transmitter circuits can be selected with a few control bits. Therefore systems could be made up of ICs from different generations.
- Interference issues: The proposed differential current mode signaling has less disturbances and interferences than the commonly used CMOS digital signaling using single-ended voltage mode signals with rail-to-rail levels and fast edges.
- Partitiong issues: The proposed low interference signaling scheme enables digital signaling between ICs, even in radio communications systems containing extremely weak analog signals, and therefore helps system design by allowing more optimum system partitioning.

4. How was the problem solved earlier?

I/O cells usually support only one type of signals, for example single-ended CMOS signals. Some existing I/O cells can be used as transmitters or receivers to support bi-directional signaling.

Systems often utilize digital signal links with voltage mode single-ended signals having rail-to-rail levels and fast edges. This kind of signals generate lots of disturbances and interferences.

High speed signals are sometimes transmitted in analog form. This requires that digital ICs contain analog circuitry and may lead to non-optimal system partitioning.

5. How does the invention improve earlier solutions? Advantages and disadvantages of the invention?

The proposed I/O circuitry supports single-ended and differential current mode, low swing voltage mode and CMOS signaling, and the operation mode of the presented receiver and transmitter circuits can be selected with a few control bits. Therefore ICs equipped with the proposed I/O cells could be configured to communicate with circuits having different signaling schemes and thus systems could be made up of ICs from different generations.

The proposed I/O circuitry supports differential current mode signaling which generates less disturbances and interferences than the commonly used CMOS digital signaling using single-ended voltage mode signals with rail-to-rail levels and fast edges. This low interference signaling scheme enables digital signaling between ICs, even in radio communications systems containing extremely weak analog signals, and therefore helps system design by allowing more optimum system partitioning.

In general, differential signaling schemes have the disadvantage of requiring two wires per signal link. This, however, mayby partially offset by the fact that differential links can support higher data rates.

The proposed multimode I/O circuitry requires some extra area. However, often I/O cells contain wide peripheral power supply buses and the standard I/O buffering is usually placed under them. Often there is extra space under the power supply buses, so the proposed circuitry may fit into the normal I/O cells.

6. Brief description of the drawings (Please enclose drawings and figures of the invention on a separate document)

- Figure 1 shows an example of the main integrated circuits and signal types in a mobile terminal. The subject of this invention report is the signaling between the circuits, and the associated I/O-cells.
- Figure 2 shows the backward (and forward) compatibily requirement, which is a necessary precondition for new signaling schemes.
- Figure 3 shows the proposed I/O-circuitry capable of multimode operation.
- Figure 4 shows the preferred mode i.e. differential current mode signaling scheme.

The following figures show how the proposed I/O-circuitry can be configured with switches to support a variety of signaling schemes.

- Figure 5 shows how the proposed circuitry can be used as two single-ended links or a single differential link, both in either current mode, low swing voltage mode or CMOS mode.
- Figure 6 shows how the proposed I/O-circuitry can be used to implement two single-ended CMOS level (rail-to-rail swing) signal links, when the supplies of the transmitter and reveiver are equal. In this mode both the receiver and transmitter can work with normal CMOS I/O-cells.

- Figure 7 shows how the proposed I/O-circuitry can be used to implement two single-ended CMOS level (rail-to-rail swing) signal links, when the supply of the transmitter is lower than that of the reveiver. NMOS transistors in series with the outputs of the transmitter stop conducting before the output voltages reach the positive supply of the transmitter and thus they protect the output transistors of the transmitter. The voltages across the terminals of these protection NMOS transistors are so low that they are not damaged. The NMOS transistors also prevent direct current flow between the positive supplies of the transmitter and receiver through the regenerative pull-up transistors. Regenerative pull-up with a weak transistor is used in the receiver to ensure sufficient signal level.

  Another way to deal with the difference in the supply voltages would be to bring the lower supply voltage of the transmitter to the receiver with an extra wire and use this lower voltage in the I/O cells of the receiver.

- Figure 8 shows how the proposed I/O-circuitry can be used to implement two single-ended CMOS level (rail-to-rail swing) signal links, when the supply of the transmitter is higher than that of the reveiver. NMOS transistors in series with the inputs to the receiver stop conducting before the input voltages reach the positive supply of the receiver and thus they protect the input transistors of the receiver. The voltages across the terminals of these protection NMOS transistors are so low that they are not damaged. The NMOS transistors also prevent direct current flow between the positive supplies of the transmitter and receiver through the regenerative pull-up transistors. Regenerative pull-up with a weak transistor is used in the receiver to ensure sufficient signal level.

  Another way to deal with the difference in the supply voltages would be to bring the lower supply voltage of the receiver to the transmitter with an extra wire and use this lower voltage in the I/O cells of the transmitter.

- Figure 9 shows how the proposed I/O-circuitry can be used to implement two single-ended current mode signal links. The receiver is configured to two transimpedance amplifiers. CMOS transmission gate is used to implement the feedback resistor.

- Figure 10 shows how the proposed I/O-circuitry can be used to implement a single differential low swing voltage mode signal link. The input drive is single-ended. Resistive load is used in the receiver to limit the signal swing. CMOS transmission gate is used to implement the load resistor. This resistor also sets the input common mode voltage.

- Figure 11 shows how the proposed I/O-circuitry can be used to implement a single differential low swing voltage mode signal link. The input drive is differential. Resistive load is used in the receiver to limit the signal swing. CMOS transmission gate is used to implement the load resistor. This resistor also sets the input common mode voltage.

- Figure 12 shows how the proposed I/O-circuitry can be used to implement a single differential current mode signal link. The input drive is single-ended. The receiver is configured to one transimpedance amplifier. CMOS transmission gates are used to implement the feedback resistors. Another CMOS transmission gate is used to set the output common mode voltage.

- Figure 13 shows how the proposed I/O-circuitry can be used to implement a single differential current mode signal link. The input drive is differential. The receiver is configured to one transimpedance amplifier. CMOS transmission gates are used to implement the feedback resistors. Another CMOS transmission gate is used to set the output common mode voltage.

7. A more detailed description of the invention (if known at the moment)

The proposed I/O cells, one transmitter and one receiver cell, which can form two single-ended links or one differential link are shown in figure 3. The various modes which these I/O cells support are shown in figures 6 to 13. A short description of each mode is given in section 6 of this document.

The proposed differential current mode signaling scheme is shown in figure 4, and the operation of this scheme is described here in more detail.

The transmitter is composed of two constant current sources (ibias1) and four switches directing the current. The signal link between ICs is composed of two adjacent wires. The receiver is composed of a differential transimpedance amplifier biased with constant current source (ibias2). Both the transmitter and receiver circuits are made up of standard MOS transistors only, as shown in figure 3.

In the transmitter the input signal controls the direction of the current flow in the signal wires by controlling the four switch transistors. The current from constant current source ibias1 is steered from one branch to another.

In the signal wires the currents have equal magnitudes but opposite directions, so the magnetic fields around the wires cancel each others in a short distance.

The receiver is a differential transimpedance amplifier composed of an amplifier and MOS feedback resistors in a shunt-shunt configuration. The differential input current is converted to a differential output voltage in this transimpedance amplifier. The input impedance of the transimpedance amplifier is very small, so the signal swing in the input, and therefore also in the whole wiring between the ICs is small.

The proposed scheme has the following advantages

- current drawn from the supplies in the transmitter is constant, ibias1. This constant current is just steered from one branch to another. This way the transmitter causes minimal disturbances in the supply lines and substrate.
- current drawn from the supplies in the receiver is constant, ibias2, so the receiver transmitter causes minimal disturbances in the supply lines and substrate.
- differential signaling in two adjacent wires radiates little electromagnetic disturbances. Signal swing in the wires is small, so capacitive coupling is low, and inductive coupling is low as well, because fields around differential wires cancel each other in a short distance from the wires.
- externally generated disturbances cause mainly common mode signal, differential signals are only caused by mismatches.
- differential wiring has lower inductance than the combination of one signal wire and a common return wire (often ground) owing to the mutual inductance. This reduces ringing in the signal lines and thereby improves noise margin and reduces timing errors.

8. Explain, how the invention is/can be implemented. Which would be the best mode of implementation?

The proposed I/O cells can be implemented using low quality MOS transistors, no other active or passive devices are needed. Therefore the scheme can be implemented in all analog, digital or mixed signal integrated circuits using digital or analog CMOS or BiCMOS technologies.

I have read and understood the invention described in this Invention Report

Date:
Signature of Manager

9. Explain how we can recognise if a competitor is using the same product/feature?

The recognition of the proposed I/O-circuitry is difficult, visual inspection with a microscope may be the only way.

10. Is it planned to use the invention in a Nokia product? If so, when and in which product? Is the invention standard related?

The invention is in idea phase but could be a potential solution for the signaling between ICs. The idea will probably be tested in a test circuit.

11. Abbreviations

ADC	analog-to-digital converter
DAC	digital-to-analog converter
IC	integrated circuit
I/O	input-output

12. Any further comments

All the presented signaling schemes, including differential current mode and low swing voltage mode signaling schemes are well known. Likewise are the good properties of the differential current mode and low swing voltage mode schemes.

The focus here is to present simple I/O-circuitry capable of multimode operation and supporting these favourable schemes. Multimode operation is important from the backward and forward compatibility point of view.

I have read and understood the invention described in this Invention Report

Date:
Signature of Manager

Code of invention:	
Opinioner:	Esa Malo

1. What device and product does the invention relate to?

The invention relates to all CMOS and BiCMOS ASIC devices.

2. What is the crystallization of invention? (What has been invented? Brief description of the key inventive feature(s))

Multimode I/O circuitry supporting many different digital data transfer protocols.

3. Is the invention new? YES/NO
If NOT new, invention is known from ...

Different dual mode and multimode I/O structures have been proposed earlier, but the ones I have seen have combined single mode structures with multiplexing possibilities (like for example DEMO-SAFARI specification).

This proposed solution combines many different modes to one receiver and one transmitter structure.

EXHIBIT B

NOKIA MOBILE PHONES, OULU, IPR

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4. Outline the merits of the invention over previous solutions?

This invention makes it more economical (smaller total silicon area) to implement multimode I/O structures compared to combination of several different single mode I/O structures. It also provides a universal CMOS based solution requiring no external components (compared to SUBLVDS) or integrated resistors.

5. What is the rating of invention? Denote with letter S after the rating value that the invention is a standard related.

5 = key strategic value (reads on the standard specification)
4 = significant (only commercially viable solution or very high potential for standard specification)
3 = moderate (difficult to design around or high potential for standard specification)
2 = modest (easy to design around or modest potential for standard specification)
1 = minor (lot of alternative implementations)
0 = none (not any interest to NOKIA, not patentable)

Rating: 2

Other comments relating the business meaning of the invention?

This invention makes it easier to combine devices with different power supply voltage or different data transfer protocol.

The final economical value can be evaluated after more detailed I/O structure design (size, power consumption, speed).

6. Suggestion to file or not to file a patent application and why?

If this idea is not already patented, it might be a good idea to file an application. If the detailed design shows that this solution gives clear economical benefits, many IC vendors might be interested in this invention.

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7. Other comments?

8. Evaluation will be sent to the inventor(s). Is it allowed to let inventor(s) know your name? (YES/NO)

yes

Date and signature	**19.4.2001 Esa Malo**

When complete, please return to:

Tiina Ojala

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Hi Harry,

1/3

Our ref: NC33004
Your ref: 872.0100 U1 (US)

Here are the documents of the "Multimode I/O circuitry supporting low interference signaling schemes for high speed digital interfaces" invention . I can also fax these documents to you if you want. This invention should be drafted during the Fall. The first draft after summer vacation, maybe during September week 38. Please confirm is that filing schedule fine?

If you have any questions please do not hesitate to ask.

BR
Tiina

> -----Original Message-----
> From: Ojala Tiina.S (NMP/Oulu)
> Sent: 18. May 2001 10:50
> To: Patent-Agency Ohlandt-OGRP (EXT-RES/Helsinki)
> Subject: Mr. Harry Smith: Inventions to filed
>
>
> Hi Harry,
>
> I have couple of inventions which should be filed during the
> Fall. Do you have time to draft these two inventions? We
> could start after summer vacation, I have my vacation in
> August. When are you on vacation?
> These two inventions are "An adaptive sigma-delta data
> converter for mobile terminals" NC32847 and "Multimode I/O
> circuitry supporting low interference signaling schemes for
> high speed digital interfaces" NC33004. Please inform me that
> could you filed those cases and your vacation times. Then I
> can send "the statement of invention" on both cases and
> inform you on drafting time schedule.
>
> BR
> Tiina
>
>

33004statement_of_inv.doc signaling6.doc signaling6.ppt expert opinion1.doc
expert opinion2.doc

7/2/01 7:12

EXHIBIT C

The purpose of the switches S1 to S12:
- S1 can be used to connect the gate of the PMOS (NMOS) transistor in the tail of the differential pair of the transmitter to ground (VDD1). This way the PMOS (NMOS) transistor turns from a current source to a small resistance, and therefore the double differential pair is effectively transformed to two separate inverters, as shown in for example Fig. 6.
- S2 can be used to connect the input i2 to a dc voltage, which is somewhere near the midway between the positive and negative supplies (the exact value is of no importance). This way a single-ended input signal can drive the double differential pair, as shown in for example Fig. 10.
- S3 can be used to connect a feedback resistor (compased of a CMOS transmission gate) between the inputs and outputs of the receiver, as shown in for example Fig. 9. This way the receiver turns from a voltage amplifier to a transimpedance amplifier with low input impedance and low input signal swing.
- S4 and S5 are extraneous and not used for anything. They are (accidental) left-overs from a mode which was removed, and therefore S4 and S5 should have been removed as well.
- S6 can be used to connect a resistor (compased of a CMOS transmission gate) in the input of the receiver to a dc voltage, which is somewhere near the midway between the positive and negative supplies (the exact value is of no importance). This reduces the imput impedance and the signal swing in the input of the receiver.
- S7 can be used to connect the gate of the PMOS (NMOS) transistor in the tail of the differential pair of the receiver to ground (VDD1). This way the PMOS (NMOS) transistor turns from a current source to a small resistance, and therefore the double differential pair is effectively transformed to two separate inverters, as shown in for example Fig. 6.
- S8 can be used to connect the gate of the PMOS, which is between the input of the receiver and VDD2, to the output of the receiver, as shown in for example in Fig. 7. This way the PMOS starts to act as a regenerative load and therefore can pull the output of the receiver all the way up to the positive supply VDD2.
- S9 can be used to connect the gate of the PMOS, which is between the input of the receiver and VDD2, to VDD2, as shown in for example in Fig. 9. This way the PMOS is shut down and no longer acts as a regenerative load.
- S10 is extraneous and not used for anything. It is an (accidental) left-over from a mode which was removed, and therefore S10 should have been removed as well.
- S11 can be used to bypass the NMOS transistors in series with the outputs of the transmitter. The series NMOS transistors are used to protect the transistors of the transmitter when the supply voltage of the receiver is higher than that of the transmitter, as shown in Fig. 7. If the supply voltages of the transmitter and the receiver are the same, the series NMOS transistors can be bypassed, as shown in for example Fig. 6.
- S12 can be used to bypass the NMOS transistors in series with the inputs of the receiver. The series NMOS transistors are used to protect the transistors of the receiver when the supply voltage of the transmitter is higher than that of the receiver, as shown in Fig. 8. If the supply voltages of the transmitter and the receiver

are the same, the series NMOS transistors can be bypassed, as shown in for example Fig. 6.

The purpose of the input nodes i1 and i2:
The transmitter can be used as a single differential transmitter, as shown in for example in Fig. 10, or two single-ended transmitters, as shown in for example in Fig. 6. In the former case the input i2 can be connected to a dc voltage with S2 and the input signal is connected to input i1. In the latter case both the inputs i1 and i2 are used and are connected to two different input signals. Fig. 4 is more conseptual in nature, the actual mode is depicted in Fig. 12 or Fig. 13. In the former figure the input is driven single-ended mode (simpler), whereas in the latter figure the input is driven differentially (symmetrical).

The operation of switches S1 to S12:
Sx = 1 means that Sx is conducting (almost short circuit), and Sx = 0 means that Sx in non-conducting (open circuit).

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Email: Patent@HSpatent.com

Facsimile Cover Sheet

Attention: Ms. Tiina Ojala	**From:** Harry Smith
Company Name: Nokia	**Date:** 13 September 2001
Fax Number: 011 358 71 80 47115	**Pages:** This cover sheet + 12
Your Ref. No.: NC 33004	**My Ref. No.: 872.0100.U1(US)**

Re: Drawings for Draft Patent Application

Dear Tiina:

Attached are the drawings for this case (Figs. 1-13). I emailed the text earlier. Sorry it took this long to finish the draft, but this is a difficult case.
BR
Harry

EXHIBIT D

* * * TRANSMISSION RESULT REPORT(IMMEDIATE TX) (SEP. 13. 2001 7:19PM) * * *

FAX HEADER: HARRINGTON & SMITH

DATE	TIME	ADDRESS	MODE	TIME	PAGE	RESULT	PERSONAL NAME	FILE
SEP. 13.	7:16PM	+358 7180 47115	G3ES	2'16"	P. 13	OK		082

# :BATCH	C :CONFIDENTIAL	$:TRANSFER	P :POLLING
M :MEMORY TX	L :SEND LATER	@ :FORWARDING	E :ECM
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* :PC	+ :ROUTING	Q :RECEPT. NOTICE REQ.	A :RECEPT. NOTICE